REMARKS

Claims 1 and 14-30 are currently pending in the application. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each .

STATEMENT OF INTERVIEW

The Examiner's consideration in an interview with the undersigned and the inventor on June 2, 2005, is acknowledged with appreciation. The interview addressed the substance of matters presented in the inventor's Article 132 Declaration previously filed. In that interview the inventor, James W. Adkisson, explained that the invention required epitaxial growth, as claimed, and the Doyle reference did not disclose epitaxial growth. On that basis the Examiner indicated that the rejection based on the Doyle prior art reference would be withdrawn. The Examiner indicated that there might be new art, and that a new art rejection would be provided upon Applicant's submission of arguments.

For completeness of the record, the following arguments are made in response to the office action mailed on 03/18/2005.

The Examiner has maintained rejection of claims 1, 14-19 and 22-30 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2003/0006410 to Doyle. In particular, in response to the applicant's amendment to the claims accompanying the RCE, the Examiner cites ¶34 on page 2 of the Doyle reference. However, as further explained below, there is no reference to epitaxial growth in Doyle, either in ¶34 or anywhere else in Doyle. Since the epitaxial limitation is patentably significant, being distinct from the amorphous layering described by Doyle as further explained below, Doyle cannot serve as a §102 reference. Nor, for the reasons also further described below, does Doyle's disclosure suggest use of epitaxial

growth. Consequently, it is believed that Doyle is overcome as a reference, and that the claims in their current form should be allowed and the case passed to issue.

Doyle describes a method of forming a quantum wire gate device, including patterning an oxide upon a substrate, forming a nitride spacer mask upon the oxide, forming an oxide spacer mask upon the nitride spacer mask, forming a further nitride spacer mask upon the oxide spacer mask, forming a plurality of channels in the substrate aligned to the further nitride spacer mask, forming a dielectric upon the channel length, and forming a gate layer over the plurality of channels (see Abstract).

The primary difficulty with the Examiner's use of the Doyle reference is that Doyle does not say anything about epitaxial layers. As shown by the Declaration of James Adkisson under Article 132, of record in the case, the term "epitaxial" has a meaning well known in the art, and refers to crystalline growth structures upon a substrate having a crystalline structure. This provides certain characteristics advantageous to the present invention, as further detailed below. By contrast, the Doyle reference uses amorphous oxides, and is unconcerned about the problems addressed and solved by the present invention. The term "epitaxial" necessarily implies a crystalline growth upon a crystalline surface.

The present invention, as summarized at page 10, lines 19-24, provides

> "a very thin diffusion region using a known technique for growing **epitaxial** regions to form the very thin channel and has the advantages of providing much tighter tolerances on channel thickness than a lithographically defined channel which can be maintained by selective etching and that **epitaxial** growth is not complicated by the presence of thin confining layers." (emphasis supplied)

This is accomplished, as summarized at page 10, lines 13-18, by the steps of

> "forming silicon layers on a substrate. Next, **epitaxial** channels are formed on a side surface of the silicon layers, with one side wall of the channels therefore being exposed. The silicon layers are then removed, thereby exposing a second sidewall of the **epitaxial** channels. Source and drain regions are then formed, coupled to ends of the **epitaxial** channels. Finally, a gate is formed over the **epitaxial** channels." (emphasis supplied)

The claim language may be understood by reference to Fig. 2C (showing the formed epitaxial layers 204 on either side of silicon layer 110), Fig. 3B (showing spacer 302 protecting a side of one 204 layer from attack), and Fig. 4B (showing the situation after removal of the other 204 layer and removal of silicon layer 110, where the second side of the first 204 layer is exposed).

It will be observed that inventor James Adkisson, who provided the Article 132 Declaration that is of record in the case, has expertise in semiconductor technology and, in particular, **epitaxial growth** at the PhD level.

Doyle is using Sidewall Image Transfer (SIT) to mask narrow channels in the silicon. That is, his channels are all below the surface of the original oxide steps (item 14 in Figs 1 and 2). To do this, he deposits nitride layers (item 16) as etch mask layers in Figs 1b and 2b (see ¶4 of the Declaration). The nitride layers (item 16) are amorphous dielectric layers. These amorphous depositions lack the crystalline properties of epitaxial depositions (see ¶5 of the Declaration). The technical meaning of "epitaxial" is very specific and requires crystalline growth, as shown in the definition attached to the Article 132 Declaration:

> epitaxy: process by which thin layer of single-crystal material is deposited on single-crystal substrate; epitaxial growth occurs in such way that the crystallographic structure of the substrate is reproduced in the growing material; also crystalline defects of the substrate are reproduced in the growing material.

The claims of the present invention are limited to use only epitaxial growth for a number of reasons (see ¶7 of the Declaration). First, the inventors want the carrier transport channels to be nearly perfect for optimum electron transport. The purpose of this method is to allow band-gap tailoring of the channel (for optimum charged-carrier transport) and well-controlled widths for the channels; epitaxy is a good method to do this. To remove them (as Doyle removes his nitride layers) would defeat the idea of the present invention.

Doyle does not perform epitaxial growth, and in fact teaches away from the use of epitaxial growth by describing nitride layers, which are amorphous dielectrics and not semiconductor crystals. The use of epitaxy, as in the definition above, assumes a crystalline layer which is perfectly, or essentially perfectly, aligned to the original material, which is itself a crystalline material (see ¶8 of the Declaration). In addition, Doyle's layers are used as sacrificial etch masks, whereas the layers we grow epitaxially are used as the conductive channels. Doyle's layers are neither present after the process is complete, nor could they be since they are not effective conductors (see ¶9 of the Declaration). Further, what the examiner points to in his review of claim 15 as semiconductor lines (item 14, in Fig. 2a of Doyle), which are necessary to form a crystalline template, are in fact oxide lines. By definition, these oxide lines are amorphous, without crystalline structure. Therefore, it makes no sense to compare them to the semiconductor lines referred to in claim 15. They clearly are not the single crystal substrate required for epitaxial growth (see ¶10 of the Declaration).

For the foregoing reasons it is submitted that the Doyle reference has been overcome as a ground for rejection.

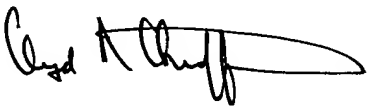
The Examiner has rejected claims 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Doyle as applied to claims 14-19 and 22-23. However, since claims 20 and 21 depend from claim 14, shown above to be in allowable form, claims 20 and 21 are also allowable.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1and 14-30 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: clyde@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account 09-0456 (IBM-Burlington).

Respectfully submitted,



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